Integrating Multiple Resistive Memory Devices on a Single Carbon Nanotube

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Nano-objects would be of great interest for the development of new types of electronic circuits if one could combine their nanometer scale with original functionalities beyond the conventional transistor action. However, the associated circuit architectures will have to handle the increasing variability and defect rate intrinsic to the nanoscale. In this context, there is a very fast growing interest for memory devices, and in particular resistive memory devices, used as building blocks in reconfigurable circuits tolerant to defects and variability. It was recently shown that optically gated carbon nanotube field effect transistors (OG-CNTFETs) based on large assemblies of nanotubes covered by an organic photoconductive thin film can be operated as programmable resistors and thus used as artificial synapses in circuits with function-learning capabilities. Here, the potential of such approach is evaluated in terms of scalability by integrating and addressing several individually programmable resistances on a single carbon nanotube. In addition, the charge storage mechanism can be controlled at a length scale smaller than the device length allowing to also program the direction in which the current flows. It thus demonstrates that a single nanotube section can combine all-in-one the properties of an analog resistive memory and of a rectifying diode with tunable polarity.

1. Introduction

New challenges in nanoelectronics do not concern the improbable ability to reproduce the performances of conventional silicon-based devices but increasing importance is given to nanodevices that can bring new functionalities through unconventional circuit architectures integrating heterogeneous technologies.[1,2] In the recent years, several examples of circuit architectures were proposed which take benefit of the high potential of nanodevices in terms of functionality and scalability.[1–5] Most of these architectures are either programmable or adaptive ones and are usually based on the combination of nanodevices with conventional electronics. In the envisioned schemes, the required nanodevices are not simply scaled-down transistors but also include memory field-effect transistors (FETs),[6–8] memristive devices,[9–13] and diodes.[14–22] In this context, resistive memory devices have a high potential notably because they can be densely integrated in crossbar arrays.[16,17,22] However, avoiding sneak paths (unwanted current pathways through non-targeted devices in neighboring rows and lines within the crossbar[21,22]) usually requires adding selection transistors and/or rectifying devices (diodes) thus increasing the process complexity and making the design less relevant in terms of integration. Devices combining programmable resistance and rectifying behavior are thus very attractive.

Among memory devices, optically gated FETs are of special interest. These light-sensitive transistors combine a semiconducting (or semi-metallic) channel such as carbon nanotubes (CNTs),[23–30] graphene,[31] nanowires,[32,33] or polymers[34] with a light-sensing material (polymers,[23–28,31,32] DNA,[29] C_{60}-derivative,[33] nanocrystals[30,34]). Among them optically gated carbon nanotube FETs (OG-CNTFETs) show the highest level of performance. In particular, we showed that devices based on large networks of randomly oriented single-walled CNTs (SWNTs) can be used as programmable resistors[28] and proposed strategies to use such CNT-based resistors as artificial synapses in circuits with function-learning capabilities.[8,35] Recently, we demonstrated that prototype circuits including 8 CNT-network

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devices can be trained (and retrained) to perform any three-input linearly separable logic function.[36] CNT networks[37–45] have a high potential for the future integration of carbon nanotubes in electronics: they are robust, little sensitive to inhomogeneity at the material level and are compatible with low-cost/large-area techniques and flexible substrates. However, CNT networks have micrometer-scale sizes and do not fully benefit from the exceptional properties of their nano-scale building blocks. At the single device level, OG-CNTFETs were built from individual CNTs[24,46] and the scaling of their programming efficiency was studied.[46] In this article, we demonstrate that multiple memory elements can be integrated on a single carbon nanotube without the need for individual gate electrodes. Several sections of the same CNT can store different values of resistance which can be adjusted independently using a combination of local signals (applied on the drain electrodes) and global signals (applied on a shared gate electrode). In addition, we evaluate the length scale at which the stored charges are controlled and show that such control allows selecting in which direction the current flows through the memory elements. It thus demonstrates that a single nanotube section can combine all-in-one the properties of an analog resistive memory and of a diode with tunable polarity.

2. Optically Gated Carbon Nanotube Field-Effect Transistors as Resistive Memories

We first summarize briefly the operating mode of conventional OG-CNTFETs and then turn to the specificities of the proposed strategy. An OG-CNTFET is composed of a CNT-based transistor channel and a light absorbing layer (usually a thin film of poly(3-octylthiophene) in this case) as schematically presented in **Figure 1**a. The channel can be either a single SWNT or a random network of SWNTs. Upon illumination, photo-generated electron-hole pairs are created in the polymer layer. At positive gate bias (V_G), part of these excitons dissociates and holes get depleted from the device while electrons are trapped in the gate dielectric close to the CNT/SiO_2 interface. The trapped electrons apply a strong negative potential to the nanotube which sets the transistor channel in its lowest resistance state (R_{ON}). When light is turned off, a significant part of the trapped electrons remains stable and are responsible for a non-volatile memory behavior. In the dark, bias pulses applied to the gate[24] or to the drain[28] electrode can then be used to adjust the density of trapped electrons and to tune the channel resistivity within a large range (more than two orders of magnitudes).[28]

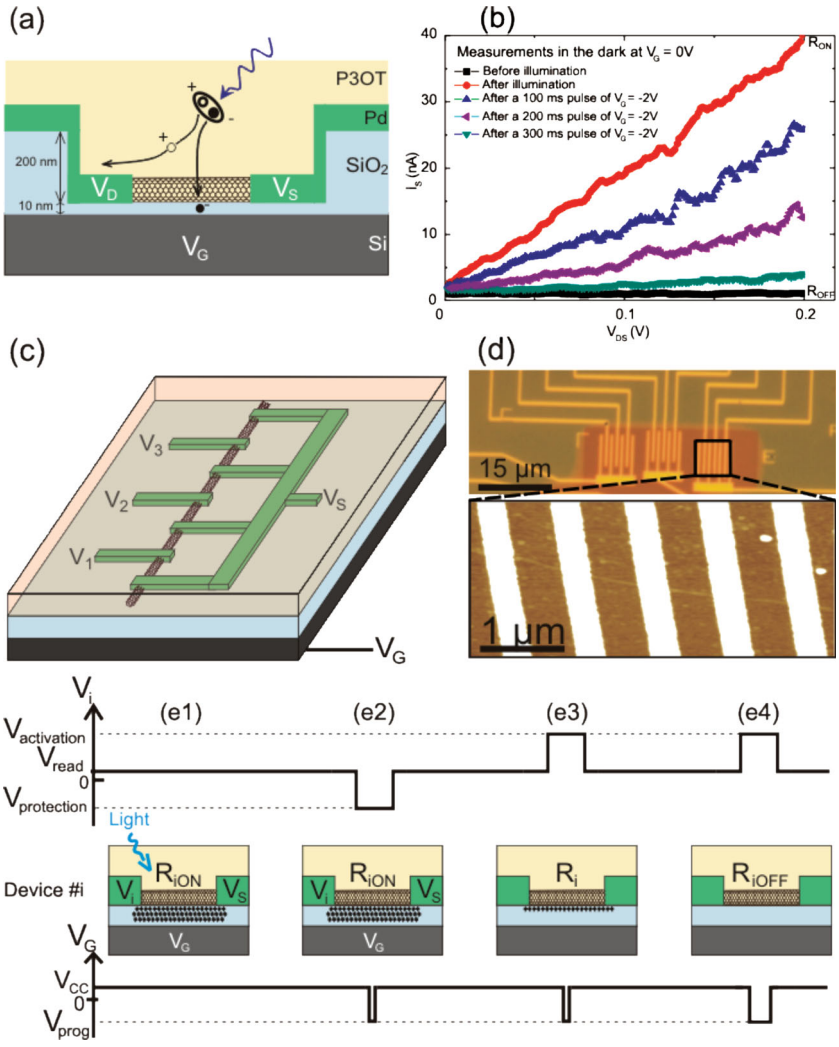

Figure 1. a) Schematic representation of an OG-CNTFET. b) Example of electrical programming of the nanotube resistivity. Before illumination, the device is in its off-state at V_{CC} = 0 V and $R_{OFF} \approx 800$ MΩ. After a 100 ms light pulse, the device is placed in its low resistance state $R_{ON} = 5$ MΩ. Then, different resistance values are programmed by applying $V_{prog} = -2$ V pulses. c) Schematic of a multi-connected SWNT forming three memory devices, each being composed of two CNT sections. The output terminals are connected to the same V_S electrode. d) Optical microscope (top) and AFM (bottom) image of an individual SWNT multi-connected. e) Principle of the programing/protection protocol. e1) After light illumination, the device #i is placed in its lowest resistance state R_{iON} at $V_G = V_{CC}$. e2) Applying a negative $V_i = V_{protection}$ prevents the negative $V_G = V_{prog}$ pulse to affect the trapped charges. e3) A resistance value R_i can be programmed by applying a combination of positive $V_{activation}$ and negative V_{prog}. e4) The device #i can be fully erased (to $R = R_{iOFF}$) by de-trapping all charges applying the combination $V_{activation}$ and V_{prog} during a longer time.

Note that in the case of multiple devices (or here multiple sections of the same CNT), light is applied globally (not locally on each device or section) and only once to set all the devices in the most conductive state. The programming itself is then electrical only, not optical.

Figure 1b illustrates the possibility of adjusting the resistivity of a SWNT between R_{OFF} and R_{ON}. Before illumination, the gate bias is first set to a positive value $V_G = V_{CC}$ (for closed channel

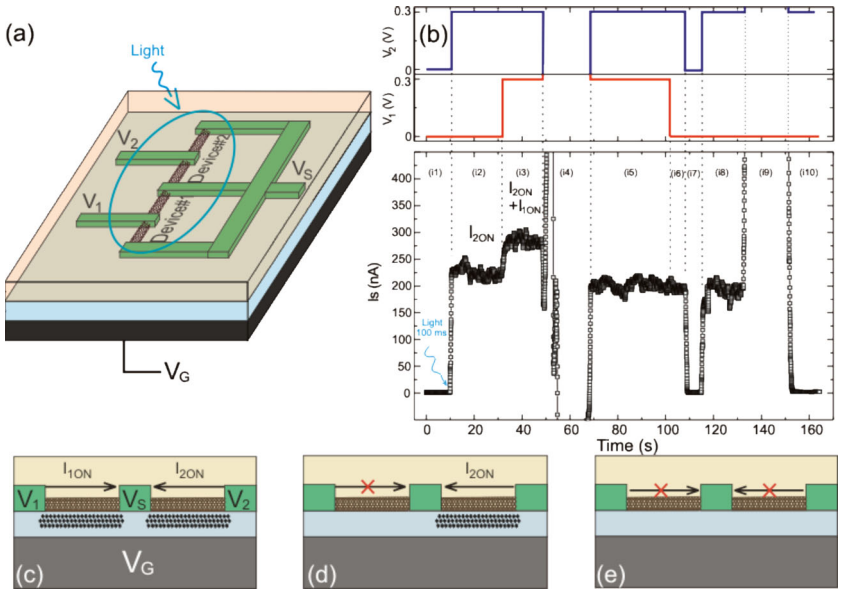

Figure 2. a) Schematic representation of the two-devices experiment. Light is applied to both devices during 100 ms so as to turn both devices in their lowest resistance state. V_G is used to program/erase the unprotected device. b) Independent programming of two neighboring devices. The current is monitored while a sequence of V_1, V_2 and V_G biases is applied. During steps (i4) and (i9), $V_{prog} = -2$ V, $V_{protection} = -2$ V and $V_{activation} = +1.4$ V so as to fully erase the unprotected device while protecting the other one from being modified. c) Schematic of the devices after illumination (only two CNT sections are represented for clarity). Photogenerated charges are uniformly trapped into the silicon dioxide. d) After erasing device #1, all the current flows through device #2. e) After erasing device #2, both devices are OFF.

voltage), which sets the transistor in its off-state so that the CNT resistance is maximal ($R_{OFF} \approx 800$ MΩ). Here, the channel was an undoped nanotube forming a normally OFF transistor and then $V_{CC} = 0$ V. However, V_{CC} is rarely 0 V and in the following of this paper (**Figure 2–5**) this gate value is $V_{CC} = 1$ V. After a light pulse (100 ms), the resistance measured in the dark is divided by a factor ≈160 to reach $R_{ON} = 5$ MΩ. Then the resistance can be programmed to any intermediate value by applying negative gate bias pulses ($V_G = -2$ V while $V_{DS} = 0.2$ V) of increasing length (here 100 ms, 200 ms and 300 ms). The efficiency of such programming depends on the magnitude of the pulses and on the gate dielectric thickness so that for a very thin (<3 nm) gate dielectric, sub-microsecond pulses are sufficient.[46] In the above example, the back-gate bias is used as programming signal so that multiple devices on the same wafer would be jointly modified. In the following, we aim at selectively address several sections of the same nanotube using combinations of source-drain and gate biases. For that purpose, we fabricated multiple electrodes on long SWNTs according to the design presented in Figure 1c. Such configuration includes three memory elements; each of them being composed of two neighboring sections (electrically wired in parallel) connected on one side by V_i ($i = 1$ to 3) and on the other side by the shared output terminal V_S. This configuration was chosen because the output current I_s directly realizes the sum of the input signals V_i multiplied by the conductance values ($1/R_i$) and is thus the simplest implementation of the synaptic part of an elementary perceptron.[8] Figure 1d displays an optical microscope image of three such structures (9 memory devices or 18 SWNT sections). Wafers were first prepared with pre-patterned areas of different oxide thicknesses: 200 nm thick oxide below the macroscopic contact pads and 10 nm thick oxide in the active area so as to limit gate leakage currents while insuring high gate efficiency. Very long (>20 µm) and straight SWNTs were grown by chemical vapor deposition on quartz substrates and transferred to the wafers (see Experimental Section for details on the growth and transfer methods). A scanning electron microscopy (SEM) image of the transferred SWNTs is presented in the Figure S1 (Supporting Information). A step of electron-beam (e-beam) lithography was used to fabricate electrical contacts and a second one to remove unwanted nanotubes outside protected areas (dark-orange area in Figure 1d, see Experimental Section). Atomic force microscopy (AFM) images confirm the presence of individual CNTs.

As mentioned above, two types of signals can be used to de-trap electrons from the SiO_2 layer: i) negative V_{prog} pulses on the gate as used in Figure 1b or ii) positive V_{prog} pulses on

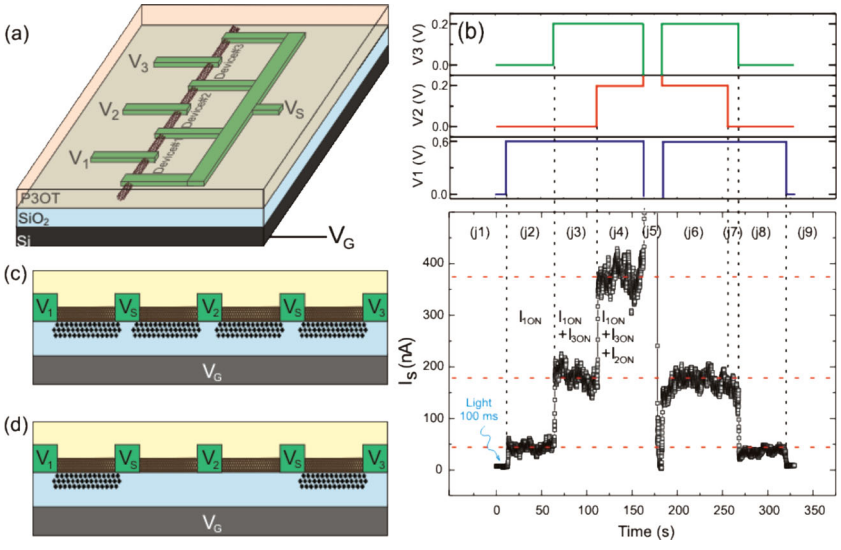

Figure 3. a) Schematic representation of the three-devices experiment. b) Independent programming of the central device #2, while devices #1 and #3 are protected from being modified. At step (j5), $V_G = V_{prog} = -2$ V, $V_1 = V_2 = V_{protection} = -2$ V and $V_3 = V_{activation} = +1.4$ V so as to fully erase the unprotected device. c) Schematic representation of the circuit after illumination. Device #2 is represented with its 2 CNT-sections while only one CNT-section of device #1 and device #3 are represented for clarity. d) Situation after the selective erasing of device #2.

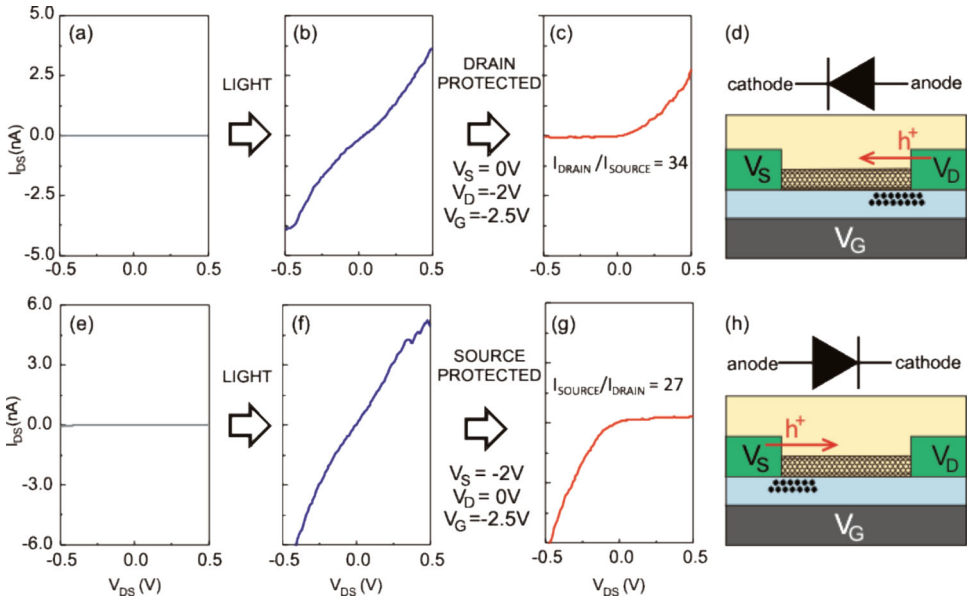

Figure 4. SWNT-based diode with reversible polarity. I_{DS} (V_{DS}) characteristics of an OG-CNTFET a) before illumination, b) after illumination, and c) after a programing protocol resulting in electrons principally trapped close to the drain electrode. d) Schematic representation of the resulting diode. e–h) I_{DS} (V_{DS}) characteristics and schematic representation of the same device but for a programming protocol resulting in electrons principally trapped close to the source electrode. Associated band diagrams are presented in the Supporting Information. All curves are recorded at V_G = 1 V and in the dark.

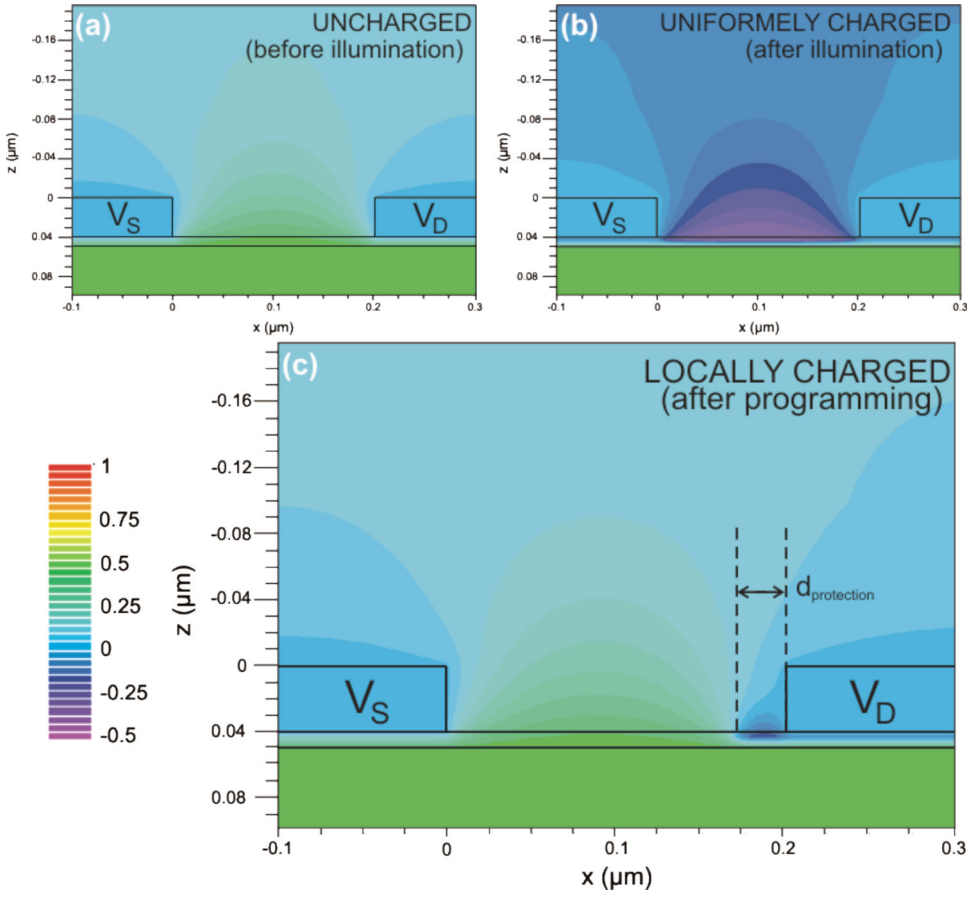

Figure 5. Electrostatic simulation of the potential distribution in the device structure at V_G = 1 V. For clarity V_S and V_D are set to 0 V. a) Initial step with no charges, b) with trapped electrons in the SiO_2 between 2 and 4 nm below the surface, and c) after the programming protocol (V_S = 0 V, V_D = $V_{protection}$ = –2 V and V_G = V_{prog} = –2.5 V). In the latter case, trapped electrons are removed from the whole device area except within a distance $d_{protection}$ ≈ 30 nm from the right contact.

the input (drain) electrode as described elsewhere.[28] However, the latter option was only applied to large CNT networks, not individual nanotubes. Indeed, applying large programming pulses on the drain electrode of a single CNT would lead to its electrical breakdown.[47] To circumvent this issue, we propose to use combinations of local V_i and global V_G biases. The different combinations of V_i and V_G signals and their impact on the trapped charges are schematically described in Figure 1e in the case of a single CNT section. The gate bias is first set to a positive value $V_G = V_{CC}$, which sets the transistor in its off-state so that the CNT resistance is maximal (R_{iOFF}). Light is then used to saturate all trap states with electrons leading to a minimal resistance state R_{iON} (Figure 1e1). In this configuration, if a negative pulse is applied to the gate ($V_G = V_{prog}$) while an also-negative pulse is applied to the drain electrode ($V_i = V_{protection}$), the situation remains unchanged since no electric field acts on the trapped electrons (Figure 1e2). Conversely, if the V_G pulse is negative and the simultaneous V_i pulse is positive ($V_i = V_{activation}$), part of the trapped electrons are released and the CNT resistance increases from R_{iON} to R'_i (Figure 1e3). Depending on the V_{prog} pulse length, arbitrary resistance values can be set by tuning the density of trapped charges, all the way to R_{iOFF} in Figure 1e4. To measure the state of a CNT section in-between programming sequences, a small and constant positive $V_i = V_{read}$ bias is used.

3. Programming Multiple Bits on a Single CNT

A central question to this work is to know whether such a strategy can be applied to multiple sections of the same SWNT and if appropriate combinations of V_1, $V_2 \ldots V_n$, V_G bias pulses allow the independent programming of each element while preserving the already programmed states. We first consider the case of two neighboring devices as sketched in Figure 2a. Figure 2b displays the evolution of the output current I_S in different configurations labeled (i1) to (i10) in the following. During (i1) light is applied to both devices while $V_1 = V_2 = 0$ V and $V_{CC} = 1$ V. We suppose a uniform density of stored electrons in the SiO_2. Theses electrons apply a negative potential to the nanotube channel placing both devices in their lowest resistance state R_{1ON} and R_{2ON} and allowing I_{1ON} and I_{2ON} to flow through device #1 and device #2, respectively. In Figure 2c is sketched the situation after such a light illumination. As the situation is similar in both CNT sections belonging to the same device, only one section per device is sketched for clarity. To evaluate these resistance values we first apply $V_2 = V_{read} = 0.3$ V in (i2) while V_1 is kept at zero. We then apply $V_1 = V_2 = V_{read}$ in (i3). At that point, we aim at fully erasing device #1 while protecting device #2. To do so, we apply jointly during (i4): $V_1 = V_{activation} = 1.4$ V, $V_2 = V_{protection} = -2$ V and a pulse of $V_G = V_{prog} = -2$ V on the gate. During (i5), we come back to the same bias condition as in (i2) where obviously the current level has been lowered from $I_{1ON} + I_{2ON}$ to a level $\approx I_{2ON}$. To actually verify that the measured I_S current flows through the device#2 only, we switch-off V_1 in (i6) and observe no change. Device #1 has been correctly set in its off-state as sketched in Figure 2d. The fact that all current flows through device #2 is further confirmed during (i7) when V_2 is switched off. At that point, we finally need to show that device #2 can also be erased with the same protocol. We first read again the R_{2ON} value in (i8) by applying $V_2 = V_{read}$. And then apply in (i9): $V_2 = V_{activation} = 1.4$ V and $V_G = V_{prog} = -2$ V. In (i10), $V_2 = V_{read}$ confirms that device #2 has been correctly erased and that no more trapped electrons affect the nanotube conductance as sketched in Figure 2e. Note that for clarity, we only described the case of a full reset of each device, which corresponds to the most demanding case (in terms of stability of the protected device). Stabilizing intermediate states without modifying the neighboring device can be achieved by simply decreasing the length of the V_{prog} pulse.

The programming protocol used above could be generalized to an arbitrary number of sections of the same nanotube if, in a series of three devices, the central one could be erased while both its neighbors remained unaffected. Such configuration is presented in Figure 3 where the sequence of applied biases is labeled from (j1) to (j9). Similarly to Figure 2, we start by evaluating the three R_{iON} values in (j1) to (j4) and then, in (j5), we erase device #2 while protecting #1 and #3 ($V_1 = V_3 = V_{protection} = -2$ V, $V_2 = V_{activation} = 1.4$ V, with a $V_G = V_{prog} = -2$ V pulse). In (j6) we show that while the biases are similar to (j4), I_S has decreased and the next sequences (j7–j9) show that the difference comes from the fact that device #2 is now fully OFF. This first part of the study thus shows that a precise selection of bias combinations allow the independent programming of different resistance values on neighboring sections of the same SWNT.

4. Local Control of Trapped Charges to Form Diodes

Up to here, the density of trapped charge below a given section of CNT was assumed to be homogeneous and the current direction was always measured in the same direction. But in fact, the control of the local trapped charge density along a SWNT can be achieved more precisely, thus allowing the study of rectifying diodes with adjustable polarity. Diodes are essential building blocks in arrays of memory devices since they can limit the issue of so-called sneak-paths in the addressing of individual devices in dense structures.[21,22] They could thus contribute to both an increased functionality and reduced power consumption.

In Figure 4, we considered an OG-CNTFET with a 200 nm long channel. Figure 4a displays the $I_{DS}(V_{DS})$ characteristics in the dark and at a constant positive gate bias ($V_{CC} = 1$ V). In such configuration, the device is in its fully off-state and no current flows through the nanotube regardless of V_{DS}. After an optical preset step, the device is placed in its fully on-state as shown in Figure 4b. The $I_{DS}(V_{DS})$ characteristic is symmetric with respect to the origin: the current value does not depend on the electrode from which charge carriers (holes in such p-type device) are injected into the nanotube. In this configuration of saturated trapped states, the biases applied on the source, drain and gate electrodes can be used to act on the spatial distribution of the trapped charges. Figure 4c displays the $I_{DS}(V_{DS})$ characteristic after a comparable programming protocol as the one used in Figures 2 and 3: a gate bias pulse of $V_{prog} = -2.5$ V is applied with the source electrode grounded ($V_S = 0$ V) and the potential on the drain electrode maintained at $V_D = -2$ V.

Such situation results in a strongly affected $I_{DS}(V_{DS})$ characteristic showing a significant rectifying behavior. The asymmetry of the output characteristic in Figure 4c demonstrates that the source and drain electrodes can be respectively associated with the cathode and anode of a diode with a rectification factor of 34 for $V = \pm 0.5$ V. The programming affects the spatial distribution of trapped electrons at a length scale smaller than the channel length, resulting in configurations where one side of the nanotube is located above trapped charges while the other side is located above a non-charged region as sketched in Figure 4d. Figure 4e–h show that the same programming protocol can be used with the same nanotube device to prepare a rectifying diode of opposite polarity by applying a protecting bias of $V_S = -2$ V on the source and $V_D = 0$ V on the drain. Such rectifying configurations, once prepared, remain stable in a significant bias range. Thus, this protocol allows the programming, at a post-fabrication step, of nanotube memory devices with an adjustable rectifying behavior.

We finally address the question of the spatial resolution of the de-trapping mechanism. Electrostatic simulations of the device structure without the nanotube were performed using Atlas version 5.16.3R from Silvaco. The simulations reproduce the potential distribution inside the device placed in the dark and biased in static conditions. The device dimensions were accurately respected in order to correctly reproduce the fabricated structures. The mesh was carefully refined in the device active area and in the oxide. Boltzmann statistics were used for the simulation, while Poisson's equation is solved by Atlas to obtain the potential distribution. Due to the device dimensions and the low charge mobility in P3OT, both leakage currents and current through the polymer can be neglected.

The simulations are performed as follows: we first compute the potential map before illumination at $V_G = V_{CC} = 1$ V, $V_S = V_D = 0$ V. As expected, we see from Figure 5a that with the thin gate oxide we use (10 nm), the potential in the centre of the device is fully set by the gate bias (note that the bias on the source and drain electrodes is set to 0 V in Figure 5 for clarity but additional potential maps at $V_D = -0.5$ V and 0.5 V are presented in the Supporting Information, Figure S2). We then simulate the effect of a light pulse by adding fixed negative charges in the oxide with a density of 2×10^{12} cm^{-2} at a depth between 2 and 4 nm from the top surface. This trapped charge density was chosen to fully screen the gate bias and to correspond to the experimental situation of Figure 1e1 where the trapped charges set the device in the on-state even though $V_G = V_{CC}$ is positive. We see in Figure 5b that in such a configuration, the potential in the centre of the device is now set by the trapped electrons while the gate bias has little effect. Next, to determine the length scale at which the protection (against de-trapping) takes place, we map the electric field in two configurations: i) $V_G = V_{prog} = -2.5$ V, $V_S = V_D = 0$ V and ii) $V_G = V_{prog} = -2.5$ V, $V_S = 0$ V, $V_D = -2$ V. The first configuration is known experimentally to fully remove all trapped charges. The second one corresponds to the local programming configuration. From this comparison, we find that for a 200 nm electrodes separation, charges are maintained trapped up to a protection length $d_{protection} \approx 30$ nm from the electrode kept at –2 V (see Supporting Information and Figures S3–S6 for details on the extraction of this distance). We then compute the potential map at $V_G = V_{CC} = 1$ V after programming (Figure 5c). Above the area where charges remained trapped (drain contact), the positive gate bias has no effect and a CNT section there would be electrostatically p-doped (i.e., in a conductive state). Conversely, the remaining length of the CNT lying on the uncharged region would be in an undoped (intrinsic) state due to the positive gate bias. The impact of such a potential profile along the SWNT on the $I_{DS}(V_{DS})$ characteristics is presented in Figure S7,S8 (Supporting Information). It is important to note that the rectifying behavior is a specificity of individual SWNTs. It would not be observed with large CNTs networks as the one used in ref. [28]. Indeed, in CNT networks, transport is diffusive and it is enough to have one side of the network in the off-state to set the full device in a high-resistance state. Conversely, in CNT-FETs based on individual SWNTs, the performances are dominated by the efficiency of carrier injection from the electrodes (hole injection from the source in p-type FETs).[48] In such a case, the presence of a resistive section of a CNT does not impair the current flow in one direction. From an integration point of view, Figure 5c suggests that downscaling the channel length to ≈60 nm (twice the $d_{protection}$ length) while preserving the rectification properties is foreseeable. Further scaling of the device length would require the combined aggressive scaling of the oxide thickness and would most probably be limited by the difficulty to insure an abrupt band profile modulation along the channel at that scale.

5. Conclusions

In conclusion, we demonstrated the feasibility of programming multiple memory devices on individual SWNTs without the use of individual gate electrodes by exploiting combinations of protection/activation/programming signals. Since the protection and activation signals are applied on the input electrodes and the programming signal is applied globally to all devices, the proposed strategy is compatible with the neural network circuit architecture presented elsewhere.[8] The use of ultralong and parallel SWNTs is also a decisive advantage for the future realization of arrays of such nanosynapses. Moreover, a SWNT can combine all-in-one the properties of an analog resistive memory and of a rectifying diode with tunable polarity. This rectifying behavior could prove very useful in solving the issues of sneak path currents in crossbar arrays of devices.

6. Experimental Section

Device Fabrication: Highly doped (1–3 × 10^{-3} Ω cm) p-type silicon substrates covered with 10 nm of thermal SiO_2 were first prepared with areas of thick SiO_2 (200 nm) supporting macroscopic (Ti/Pt) contact pads. Long and aligned SWNTs were grown by catalytic chemical vapor deposition (CCVD) on quartz substrates and then transferred on these wafers according to the following protocol. ST-cut quartz substrates (Hoffman Materials Inc.) were annealed for 8 h at 900 °C in air to heal the surface defects. Catalyst line patterns (5 Å of iron) were created by photolithography and thermal evaporation. The obtained catalysts were subjected to air oxidation treatment at 700 °C for 30 min. The samples were then loaded into the CCVD tubular furnace and the temperature was ramped to 950 °C in argon at a flow rate of 1400 sccm, followed by a hydrogen reduction process for 10 min at a flow rate of 400 sccm.

After the reduction process, methane was introduced into the furnace at a flow rate of 100 sccm. The synthesis temperature was 950 °C and the growth time time 30 min. The as-grown samples were analyzed by field emission SEM (FE-SEM, QUANTA 200F, FEI). For transferring the nanotubes to the silicon substrates, we used a PMMA layer as mediator. Spin-coating process was performed by PMMA solution at 2000 rpm for 30 s on the quartz substrate with aligned SWNTs. After baking the substrate on a hot plate at 170 °C for 10 min, the substrate and PMMA film were dipped in KOH (1 M) for 15 min to make the PMMA layer peel off the quartz substrate. Then, the PMMA layer was transferred to the pre-patterned silicon substrate, dried and dissolved in acetone. Electron beam lithography was used to design V_i and V_S electrodes composed of the 0.7/7/32 nm thick Ti/Pd/Au. In order to remove unwanted carbon nanotubes on the surface that could act as short-circuits, reactive ion etching (RIE) was performed. For protecting the device from the oxygen plasma, e-beam lithography was used to prepare a PMMA/FOX12 (Sigma Aldrich) protecting mask that was then removed using acetone. The devices were finally covered with a ≈10 nm thick layer of commercial (Sigma-Aldrich) poly(3-octylthiophene) deposited from a solution diluted in toluene (0.1 wt%), spin coated at 3000 rpm and dried in air at 100 °C for 10 min.

Measurements: Electrical measurements were performed in air at room temperature. Light was applied using an Ar-Kr laser beam at $\lambda = 457$ nm focused through a confocal microscope system (spot size ≈ 3 μm^2). A single light pulse at $P \approx 100$ W cm^{-2} was applied before a programming sequence.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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